CLAIMS

What is claimed is:

1. A variable attenuator for controllably attenuating an AC signal comprising:

a plurality of alternate series and shunt variable resistors coupled between a variable attenuator input and a variable attenuator output, each variable resistor having at least one field effect transistor (FET) having a body, a source, a drain and a gate, with parasitic capacitances between the gate and source, the gate and drain, the source and body and the drain and body, the parasitic capacitances providing respective parasitic impedances at the frequencies of the AC signal;

the body of each FET being coupled to a circuit reference through a respective resistance having an impedance higher than the parasitic impedances to the body;

the gate of each FET being coupled to a respective control voltage through a respective resistance having an impedance higher than the parasitic impedances to the gate;

each FET being biased to operate in its linear region; and

a FET gate control circuit controlling the gate of each field effect device responsive to an attenuator control signal, the FET gate control turning on the FETs in the shunt

variable resistors and turning off the FETs in the series variable resistors progressively and at predetermined rates to monotonically increase the attenuation of the AC signal from a minimum to a maximum attenuation, and turning off the FETs in the shunt variable resistors and turning on the FETs in the series variable resistors progressively and at predetermined rates to monotonically decrease the attenuation of the AC signal from the maximum attenuation to the minimum attenuation.

2. The attenuator of claim 1 wherein the reference voltage is a circuit ground.

3. The attenuator of claim 1 wherein the attenuator is a single ended attenuator.

4. The attenuator of claim 1 wherein the attenuator is a differential attenuator.

5. The attenuator of claim 1 wherein the DC source-to-drain voltages of the FETs are substantially zero.

6. The attenuator of claim 1 wherein each of the shunt variable resistors comprises a FET in series with a resistor.

7. The attenuator of claim 1 wherein each of the series variable resistor comprises a FET in parallel with a resistor.

8. The attenuator of claim 1 wherein each of the shunt variable resistors comprises a FET in series with a resistor and each series variable resistor comprises a FET in parallel with a resistor.

9. The attenuator of claim 8 further comprised of second FETs, each in parallel with a respective shunt variable resistor, each second FET being small in comparison with the FETs in the series variable resistors and each being controlled in unison with a FET in a series variable resistor.

10. The attenuator of claim 8 further comprised of second FETs, each in parallel with the FET in a series variable resistor, each second FET being small in comparison with the FETs in the shunt variable resistors and each being controlled in unison with a FET in a shunt variable resistor.

11. The attenuator of claim 8 further comprised of second FETs, each in series with a resistor, each series combination of a second FET and a respective resistor being

coupled in parallel with the FET in a respective series variable resistor.

12. The attenuator of claim 11 wherein each second FET is large in comparison with the FETs in the shunt variable resistors and each second FET being controlled in unison with a FET in a shunt variable resistor.

13. The attenuator of claim 1 wherein the FET gate control circuit comprises a voltage divider dividing a reference voltage into a plurality of lower voltage references, and a plurality of differential amplifiers, each differential amplifier providing a differential output responsive to the difference between a respective reference and the attenuator control signal.

14. The attenuator of claim 13 wherein;

each differential amplifier comprises first and second transistors, each having first and second terminals and a control terminal, the conduction between the first and second terminals being responsive to the voltage between the control terminal and the first terminal, the first terminals of the first and second transistors each being coupled to a current source through a respective resistor, the second terminals of the first and second transistors each being coupled to a

respective current mirror, each current mirror being coupled to a respective load resistor;

the voltages across the load resistors controlling the FETS in the series and shunt variable resistors.

15. The attenuator of claim 14 wherein the first and second transistors are FETs.

16. The attenuator of claim 14 wherein the first and second transistors are bipolar junction transistors.

17. A variable resistor for use with an AC signal having AC signal frequencies comprising:

a field effect transistor (FET) having a body, a source, a drain and a gate, with parasitic capacitances between the gate and source, the gate and drain, the source and body and the drain and body, the capacitances having respective impedances at the AC signal frequencies;

the body of the FET being coupled to a circuit reference through a resistance having an impedance higher than the impedance of the parasitic capacitances to the body;

the gate of the FET being coupled to a respective control voltage through a respective resistance having an impedance higher than the impedance of the gate;

the FET being biased to operate in its linear region.

18. The variable resistor of claim 17 further comprised of a resistor coupled in parallel with the FET.

19. The variable resistor of claim 17 wherein the reference voltage is a circuit ground.

20. The variable resistor of claim 17 wherein the DC source-to-drain voltage of the FET is substantially zero.

21. A π-attenuator for use with an AC signal having AC signal frequencies comprising having an input terminal, an output terminal and a common terminal comprising:

a first variable resistor coupled between the input terminal and the common terminal;

a second variable resistor coupled between the input terminal and the output terminal;

a third variable resistor coupled between the output terminal and the common terminal;

each variable resistor having a field effect transistor (FET) having a body, a source, a drain and a gate, with parasitic capacitances between the gate and source, the gate and drain, the source and body and the drain and body, the capacitances having respective impedances at the AC signal frequencies;

the body of each FET being coupled to a circuit reference through a respective resistance having an impedance higher than the impedance of the parasitic capacitances to the body;

the gate of each FET being coupled to a respective control voltage through a respective resistance having an impedance higher than the impedance of the respective gate;

the FETs each being biased to operate in its linear region.

22. The π-attenuator of claim 21 wherein the reference voltage is a circuit ground.

23. The π-attenuator of claim 21 wherein the DC source-to-drain voltages of the FETs are substantially zero.

24. The π-attenuator of claim 21 wherein the second variable resistor comprises a FET in parallel with a resistor and the first and third variable resistors each comprise a FET in series with a resistor.

25. The π-attenuator of claim 24 further comprised of a fourth and fifth FETs, each in parallel with a respective one of the first and third variable resistors, each of the fourth and fifth FETs being small in comparison with the FET in the second variable resistor.

26. The π-attenuator of claim 24 further comprised of a fourth FET in parallel with the FET in the second variable resistor, the fourth FET being small in comparison with the FETs in the first and third variable resistors.

27. The π-attenuator of claim 24 further comprised of second FETs, each in series with a resistor, each series combination of a second FET and a respective resistor being coupled in parallel with the FET in the second resistor.

28. The π-attenuator of claim 24 wherein each second FET is large in comparison with the FETs in the first and third variable resistors.

29. A T-attenuator for use with an AC signal having AC signal frequencies comprising having an input terminal, an output terminal and a common terminal comprising:

first and third variable resistors coupled in series between the input terminal and the output terminal, respectively;

a second variable resistor coupled between a node between the first and third variable resistors and the common terminal;

each variable resistor having a field effect transistor (FET) having a body, a source, a drain and a gate, with

parasitic capacitances between the gate and source, the gate and drain, the source and body and the drain and body, the capacitances having respective impedances at the AC signal frequencies;

the body of each FET being coupled to a circuit reference through a respective resistance having an impedance higher than the impedance of the parasitic capacitances to the body;

the gate of each FET being coupled to a respective control voltage through a respective resistance having an impedance higher than the impedance of the respective gate;

the FETs each being biased to operate in their linear region.

30. The T-attenuator of claim 29 wherein the reference voltage is a circuit ground.

31. The T-attenuator of claim 29 wherein the DC source drain voltages of the FETs are substantially zero.

32. A variable attenuator for controllably attenuating an AC signal comprising:

a plurality of alternate series and shunt variable resistors coupled between a variable attenuator input and a variable attenuator output, each variable resistor having at

least one field effect transistor (FET) having a source, a drain and a gate;

each FET being biased to operate in its linear region; and

a FET gate control circuit controlling the gate of each field effect device responsive to an attenuator control signal, the FET gate control turning on the FETs in the shunt variable resistors and turning off the FETs in the series variable resistors progressively and at predetermined rates to monotonically increase the attenuation of the AC signal from a minimum to a maximum attenuation, and turning off the FETs in the shunt variable resistors and turning on the FETs in the series variable resistors progressively and at predetermined rates to monotonically decrease the attenuation of the AC signal from the maximum attenuation to the minimum attenuation.

33. The attenuator of claim 32 wherein the DC source-to-drain voltages of the FETs are substantially zero.

34. The attenuator of claim 32 wherein the FET gate control circuit comprises a voltage divider dividing a reference voltage into a plurality of lower voltage references, and a plurality of differential amplifiers, each differential amplifier providing a differential output

responsive to the difference between a respective reference and the attenuator control signal.

35. The attenuator of claim 34 wherein;

each differential amplifier comprises first and second transistors, each having first and second terminals and a control terminal, the conduction between the first and second terminals being responsive to the voltage between the control terminal and the first terminal, the first terminals of the first and second transistors each being coupled to a current source through a respective resistor, the second terminals of the first and second transistors each being coupled to a respective current mirror, each current mirror being coupled to a respective load resistor;

the voltages across the load resistors controlling the FETS in the series and shunt variable resistors.

36. A variable resistor for use with an AC signal having AC signal frequencies comprising:

a field effect transistor (FET) having a source, a drain and a gate;

a resistance having a first end coupled to the source and a second end coupled to the drain;

a control signal being coupled to the gate;

the FET being biased to operate in its linear region.

37. The variable resistor of claim 36 wherein the DC source-to-drain voltages of the FETs are substantially zero.

38. A π-attenuator for use with an AC signal having AC signal frequencies comprising having an input terminal, an output terminal and a common terminal comprising:

a first variable resistor coupled between the input terminal and the common terminal;

a second variable resistor coupled between the input terminal and the output terminal;

a third variable resistor coupled between the output terminal and the common terminal;

each variable resistor having a field effect transistor (FET) having a body, a source, a drain and a gate;

the FETs each being biased to operate in its linear region.

39. The π-attenuator of claim 38 wherein the DC source-to-drain voltages of the FETs are substantially zero.

40. A T-attenuator for use with an AC signal having AC signal frequencies comprising having an input terminal, an output terminal and a common terminal comprising:

first and third variable resistors coupled in series between the input terminal and the output terminal, respectively;

a second variable resistor coupled between a node between the first and third variable resistors and the common terminal;

each variable resistor having a field effect transistor (FET) having a body, a source, a drain and a gate, with parasitic capacitances between the gate and source;

the FETs each being biased to operate in their linear region.

41. The T-attenuator of claim 40 wherein the DC source-to-drain voltages of the FETs are substantially zero.